Remarks

Continued examination and reconsideration of the subject application, as amended, is respectfully requested.

The claims of the subject application are directed to a digital signal processing apparatus and method in which, *inter alia*, independently reconfigurable processing elements in an array of independently reconfigurable processing elements are configured to perform a block cipher routine, and reconfigured during the processing to perform subfunctions of the routine.

An example of an independently reconfigurable processing element is provided in Figure 3 of the subject application. In this example, a reconfigurable cell 200 includes functional units which are activated according to the function being executed by the reconfigurable cell during a processing cycle. (See Subject Application, paragraphs 0017-0019.) The functional units can include, without limitation, a Multiply-and-Accumulate (MAC) functional unit, an arithmetic unit, and a logic unit. The functional units are configured to execute logical operations which include, without limitation, XOR, OR, AND, store, shift, and truncate. Other types of functional units for performing other functions are possible.

In the embodiment of a reconfigurable cell described in Figure 3, the functional units are controlled and activated by a context register. The context register latches a context instruction and provides the context instruction to the appropriate functional unit(s). (*See*, Subject Application, paragraph 0019.)

As a result, routines, such as a block cipher routine, can be executed with the high performance of a hardware implementation such as an ASIC, yet with the flexibility and scalability of software executed by general purpose processors. (*See*, Subject Application, paragraph 0024.)

Claims 1-41 are pending in the Subject Application, with claims 1, 21 and 31 being independent claims.

Amendments to the claims:

Although it is believed that the use of the term "configuring" in the context of "independently reconfigurable processing elements" in originally filed claims 1 and 21, and the recitation of "an array of independently reconfigurable processing elements" "being configured" in originally filed claim 31, recite the concept of changing the configuration of the processing element during the block cipher routine, these claims have been amended to more clearly recite such a feature. Specifically, claims 1 and 21 have been amended to recite "including reconfiguring the configured portion to perform subfunctions of the block cipher routine." Claim 31 has been amended to recite that the array of independently reconfigurable processing elements is responsive "for being reconfigured to perform subfunctions of the block cipher routine during execution of the block cipher routine." Support for these amendments can be found in paragraphs 0029 through 0037 of the subject application.

Certain claims of the subject application have been renumbered to address the Examiners claim objections regarding the separation of dependent claims from one another. See page 2, paragraph 2, of the Office Action. The renumbered claims are as follows:

Original	Renumbered
4	9
5	4
6	10
7	11
8	5
9	6
10	16
11	17
12	7
13	12
14	13
15	14
16	8
17	15
25	26
26	27
27	25

It is respectfully submitted that the Examiner's objection to the numbering of the dependent claims has been overcome by this amendment.

Original claim 16 (now renumbered to be claim 8) has been amended to recite "includes one or more processing elements." Support for this amendment can be found in paragraph [0017] of the subject application.

Original claim 17 (now renumbered claim 15) has been amended to recite "two or more active processing elements." Support this amendment can be found at paragraph [0030] of the subject application.

Claim 18 has been amended to recite that the data blocks received "are each 64 bits or more in length." Support for this amendment can be found at paragraph [0014] of the subject application.

Claim Rejections:

The Examiner has rejected claims 1-10, 19-25, 30-36 and 41 under 35 U.S.C. 102(e) as being anticipated by US Pat. No. 6,088,800 to Jones et al. (Official Action, p. 2.) Applicants respectfully traverse this rejection. Applicant respectfully traverses this rejection.

As explained in the Amendment, filed August 3, 2005, in Jones et al. the configuration of each of the PEs, including the ALU, is the same, although the series of instructions being executed by one PE during a process may be different from the series of instructions being executed by another PE. It is the instruction sequence which changes, not the underlying configuration of the PE.

In contrast, as illustrated in Figure 3 and described in paragraphs 0017 to 0019 of the Subject Application, for example, and more clearly recited in amended claims 1, 21 and 31, the claimed invention involves configuring and reconfiguring "independently reconfigurable processing elements." That is, the claimed invention in the context of the described embodiment, involves activating or deactivating functional units in a reconfigurable processing element by so that the combination of the activated functional units defines the operation of the reconfigurable processing element as reconfigured for

a processing cycle, rather than using an ALU of a fixed configuration, such as in Jones et al.

Although, on page 2, paragraph 1, of the Office Action, the Examiner points to the disclosure of the changing of a "key session" at col. 10, line 47 – col. 11, line 11 of Jones et al., it is respectfully submitted that such passage does not disclose the reconfiguring of the processing element being used, but rather discloses the changing of the information used in the processing.

The Examiner has cited Sorimachi, US 2002/0181709, in combination with Jones et al. in rejecting claims 11-18, 26-29, and 37-40 under 35 USC 103(a). However, the Examiner has not relied upon Sorimachi as teaching independently reconfigurable processing elements. It is respectfully submitted that Sorimachi does not teach or suggest the independently reconfigurable processing elements, and reconfiguring thereof, recited in amended claims 1, 21, and 31.

For the foregoing reasons it is respectfully submitted that claims independent claims 1, 21, and 31 are allowable, and that claims 2-20, 22-30 and 32-41, as dependent from allowable base claims, are also allowable.

Conclusion

For the above reasons it is respectfully submitted that the subject application is in condition for allowance, and the Examiner's indication to that end is respectfully solicited.

Respectfully submitted,
DLA Piper Rudnick Gray Cary US LLP

Dated: August 7, 2006 By: 

Gerald T. Sekimura
Reg. No. 30,103
Tel.: (415) 836-2500

Attn. Patent Department
DLA Piper Rudnick Gray Cary US LLP
153 Townsend Street, Suite 800
San Francisco, CA 94107-1957